REMARKS

Reconsideration of the present application is respectfully requested.

Summary of Office Action

Claims 1-39 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement and as failing to comply with the enablement requirement.

Summary of Amendments

No claims have been amended, canceled or added in this response.

Discussion of Rejections

Claims 1-39 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement and the enablement requirement. The Examiner indicates that he is unable to find support for the limitations "create an aggregate transport stream in a single format from the plurality of transport streams".

Applicants respectfully traverse, since clear and detailed support for these limitations is provided in the specification as filed at, for example, paragraphs [0028], [0046], [0062], [0068] and [0081]-[0084] and in Figures 7, 8 and 13. These paragraphs describe that the front end 410 (Fig. 4B) includes a packet processor 830 (Fig. 13), which inputs four streams from the switching matrix 820 and appends header and footer information **to create a 208-byte proprietary packet format** (Fig. 7). For example, paragraph [0068] provides:

> [0068] In one embodiment, External Input/Output 810 can receive 8 streams, which are sent to the Switching Matrix sub-block 820, where four streams are chosen (based on user configuration) to be sent to Packet Processor 830. **The Packet Processor sub-block 830 aggregates**

packets from the 4 chosen streams and writes them out to a common memory buffer for further processing. It is the Packet Processor 830 that attaches appropriate header and footer information to a transport packet. In one embodiment, the Packet Processor 830 writes the packets out in 208-byte format to Memory. To obtain bit-fields in the header and footer, the Packet Processor 830 also interfaces with Packet Counter and Timestamp sub-block 840. In one embodiment the Timestamp sub-block 840 is instantiated multiple times to allow support for multi-channel or multi-tuner receiver systems. Each Timestamp sub-block contains a counter clocked by the clock generated by an independent VCXO. The Packet Processor 830 can be programmed to choose timestamps from any one of the Timestamp sub-blocks. (Emphasis added.)

Figure 7 and paragraph [0062] describe the proprietary packet format in detail. Figure 13 and paragraphs [0081]-[0084] describe the structure and functionality of the packet processor 830 in detail.

In view of the foregoing facts, Applicants respectfully submit that the rejections are improper and request that they be withdrawn.

Conclusion

For the foregoing reasons, the present application is believed to be in condition for allowance, and such action is earnestly requested.

If there are any additional charges/credits, please charge/credit our deposit account no. 02-2666.

Respectfully submitted,
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